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PATENT

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Title: ELECTRICAL ISOLATION OF OPTICAL COMPONENTS IN
PHOTONIC INTEGRATED CIRCUITS (PICs)

AMENDMENT B

A. Claim Comparison of Claim 1 of This Application 10/807,729 Against Claim 47
of US 6,771,682 B2

Note that ~~strike-throughs~~ are only found in claim 47 of Patent '682 and underlines are only found in claim 1 of this application '729, and the rest of the claim language is the same in both claims:

1. 47. A method of electrically isolating spatially disposed semiconductor electro-optic components integrated on a substrate, ~~which are formed in a plurality of deposited semiconductor layers~~ where a first electro-optic component comprising a semiconductor laser is operated with a first bias current with a steady state condition and a second electro-optic component comprising an electro-optic modulator is operated with a second bias current with modulated variations in accordance with an electrical modulated signal applied to the second electro-optic component, comprising the steps of:

activating the electro-optic components with the first and second applied bias currents whereby an undesired parasitic current is established along a first electrical path between them via some of the semiconductor layers, the parasitic current also transferring modulated variations created at the second electro-optic component over to the first electro-optic component via the first electrical path so that the latter no longer operates in its steady state condition;

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establishing an electrical isolation region between the first and second electro-optic components to create a second electrical path transverse ~~in direction to the first electrical path and formed between a bias point at surface region of the electrical isolation region and the first electrical path between the electro-optic components~~; and

applying a bias to the bias point at the electrical isolation region to divert the parasitic current from the electrical first path through the second electrical path to the bias point resulting in divided parasitic currents, respectively, between the first electro-optic component and the bias point and between the bias point and the second electro-optic component so that the undesired modulated variations along the first electrical path are substantially eliminated from affecting the first electro-optic component.

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B. Amendments to Claim 1 in This Application 10/807,729:

1. (Currently amended) A method of electrically isolating spatially disposed semiconductor electro-optic components integrated on a substrate, where a first electro-optic component is operated with a first bias current with a steady state condition and a second electro-optic component is operated with a second bias current with modulated variations in accordance with an electrical modulated signal applied to the second electro-optic component, comprising the steps of:

activating the electro-optic components with the first and second applied bias currents whereby an undesired parasitic current is established along a first electrical path between them ~~via some of the semiconductor layers~~, the parasitic current also transferring modulated variations created at the second electro-optic component over to the first electro-optic component via the first electrical path so that the latter no longer operates in its steady state condition;

establishing an electrical isolation region between the first and second electro-optic components to create a second electrical path transverse to the first electrical path; and applying a bias at a bias point at the electrical isolation region to divert the parasitic current from the electrical first path through the second electrical path to the bias point resulting in divided parasitic currents, respectively, between the first electro-optic component and the bias point and between the bias point and the second electro-optic component so that the undesired modulated variations along the first electrical path are substantially eliminated from affecting the first electro-optic component.